IN THE SPECIFICATION

Please amend paragraph [0022] to read as follows:

[0022] FIG. 1 shows a multi-bank or multi-array memory with four memory banks 19A-19D to illustrate the basic concept of this invention. In a multi-bank or multi-array memory with several banks 19A-19D in each cycle, only one bank or array is activated for the purpose of normal memory access while one or more of the other banks are activated for the purpose of being refreshed. Therefore, during each cycle, more than one bank or array is activated simultaneously. In FIG.1 where two banks 19A/19C are activated at the same time, the first, ACCESS bank 19A is accessed for a normal read or a normal write operation, while a second, REFRESH bank 19C is refreshed. The decision as to whether or not a particular bank will be refreshed is done by a refresh scheduler book unit 13. The refresh scheduler book unit 13 manages the refresh schedule of every bank including ACCESS bank 19A, bank 19B, /REFRESH bank 19C and bank 19D or memory array and issues the global address on lines [[14]] 14A (RBA), 14B (RRA) for a refresh operation while simultaneously bypassing normal access bank address lines including BA lines 16A and RA lines 16B issued externally by the user or system to row decoders 15A, 15B, 15C and 15D. On the one hand, lines 14B carry the RBA (Refresh Bank Address) signal and lines 16A ~~carries~~ carry the BA (Bank Address) signal respectively. Also, lines 14A carry the RBA (Refresh Bank Address) signal and lines 16B carry the RA (Row Address) signal. The refresh scheduler book unit 13 sends mode selection (mode SEL) signals on lines 11 together with the refresh address RA signals on lines 16B to the row decoders 15A to 15D. The mode selection signal lines 11 carry the information as to which address the row decoder 15A/15B/15C/15D of the selected bank including ACCESS bank 19A/bank 19B/REFRESH bank 19C/bank 19D should accept. The output of the decoder 15A on WLi line 18A is connected to the input of the ACCESS bank 19C. The output of the decoder 15B on line 18B is connected to the input of the bank 19B. The output of the decoder 15C on WLj line 18C is connected to the input of the REFRESH bank 19C. The output of the decoder 15D on line 18D is connected to the input of the bank 19D.

Please amend paragraph [0024] to read as follows:

[0024] FIGS. 2A and 2B show block diagrams of key components of the system of this invention. FIG. 2A shows the connections for a single generic bank 19. In FIG. 2A, an address buffer 17 supplies the BA signals on lines 16A and the RA signals on lines 16B. Conflict signals between the address buffer 1 and an arbiter 25 are interconnected via conflict signal line 62 which connects from the address buffer and bidirectional line 62O which connects bidirectionally to the arbiter 25. A refresh scheduler book unit 13 in accordance with this invention comprises a Row ADDress MUltipleXer (Row ADD MUX) 23, up flag register FBU 21 and down flag register FBD 22, comparator block 24 and arbiter 25. A row address decoder 27, a wordline driver 28 and a Bank 19 are also shown in FIG. 2A, and the row address decoder 27, the wordline driver 28 and a Bank (n-1) 19Z ~~Bank n-119Z~~ are also shown in FIG. 2B. FIG. 2B also shows the additional banks Bank (32) 19Y and Bank (0) as part of an array of banks, as indicated by the dotted lines therebetween.

Please amend paragraph [0026] to read as follows:

[[A]] Referring to FIG. 2A, a Fixed RBA (Fixed Refresh Bank Address) register ~~(Fixed RBA)~~ 29 is a uniquely assigned bank address to the shown bank through an output line 14A connected to both the comparator block 24 and the Row ADD MUX 23.

Please amend paragraph [0029] to read as follows:

[0029] A conflict signal line 62 is connected via line 62O (shown in FIGS. 2A, 2B, and 5) to send and receive conflict signals to and from the arbiter 25.

Please amend paragraph [0031] to read as follows:

[0031] FIG. 2B shows three sets of circuits for a few exemplary banks BANK0 19X, BANK32 19Y, and bank BANK(n-1) 19Z out of n banks in an array thereof connected to lines 16A/16B and 62 as in FIG. 2A.

Please amend paragraph [0032] to read as follows:

[0032] FIG.3 shows the details of Row ADD MUX 23 of FIG.2 and Row Address Counter (RAC) 31 and its connection to the Word Line Driver 28 which provides a "WORD LINE i" output on line 28'. It is comprised of RAC (Row Address Counter) counter 31 and two multiplexers comprising an upper MUX 32 and a lower MUX 33. Both the upper MUX 32 and the lower MUX 33 in FIG.3 have a common input select signal, which is the selection signal, i.e. the Mode SEL signal on line 26 from the arbiter 25 as shown in FIGS. 2A, 2B and 6. The row decoder 27 receives an input on line 32' from the upper MUX 32 and another input on line 33' from the lower MUX 33. The row decoder 27 provides an input on line 27' to the wordline driver 28, which provides a WORD LINEi output on line 28'. The upper MUX 32 in FIG.3 selects one out of two row address inputs, one on line [[~~31~~]] 31' from RAC counter 31 and the other on RA line 16B from the address buffer 17 in FIGS. 2A and 2B. The RAC counter 31 provides the row address to be refreshed within each bank and automatically increases the row address therein after the selected bank is refreshed. The role of RAC 31 is to keep track of the refreshing process progressing from bank to bank by increasing the count in the respective RAC counter 31 whenever the bank is refreshed. The lower MUX 33 selects one bank address out of two bank address inputs, including BA input on lines 16A and RBA inputs on line 14A. The two MUX units 32/33 select the refresh address or normal address depending on the Mode SEL signal polarity on line 26 from the refresh scheduler book unit 13.

Please amend paragraph [0033] to read as follows:

[0033] The Mode SEL signal on line 26 determines whether a bank will be normally accessed or refreshed. If the incoming bank address on line 16A and the refresh bank address on RBA line 14A are the same, the Mode SEL signal on line 26 selects the incoming bank address (BA) on line 16A and row address (RA) on line 16B and the bank performs its Normal operation. On the other hand, if the incoming bank address (BA) on line 16A and the refresh bank address (RBA) on line 14A are not the same and when the decision to refresh the bank is made, the Mode SEL selects the refresh bank address (RBA) on line 14A and the RAC counter 31 provides an output via multiplexer 23 to the row decoder 27.

Please amend paragraph [0037] to read as follows:

[0037] FIG.5 shows the connections to a generic arbiter 25. The arbiter 25 is connected to receive FBU and FBD bits on line 41 and 42 in each bank, comparator result on line 44 and conflict signal on the ~~common~~ conflict signal line 62O [[62]]. The arbiter 25 generates Mode SEL and conflict signal as outputs. The conflict signal on the conflict signal line 62O [[62]] behaves as both an input and an output depending on flag bits. The arbiter 25 of a bank that has FBU "0" and FBD "1" will not take the conflict signal on the conflict signal line 62O [[62]] as an input and instead bypass the comparator result on line 44 to conflict signal line 62. On the other hand, the arbiter 25 of the bank that has FBU "1" and FBD "0" will take the conflict signal on the conflict signal line 62O [[62]] as an input without bypassing the comparator result from line 44 to the conflict signal line 62O [[62]].

Please amend paragraph [0041] to read as follows:

[0041] FIG. 6D shows a hybrid form of flowchart 71 of an algorithm, signal, and devices, in accordance with the invention and FIGS. 6A-6C, which operates as follows:

Please amend paragraph [0044] to read as follows:

[0044] FBU(n-2),...(0) = FBD(1)…FBD(n-1)=0

~~FBU(n-2),.. = FBU(0).= FBD(1)…FBD(n-1)=0~~

Please amend paragraph [0046] to read as follows:

[0046] 2. The outputs of reset block 74 on line 75 including FBU(j)=0, FBD(j)=1, FBU(i)=1, and FBD(i) =0 flow[[s]] as shown by FIG. 6D to comparator block(i) 24i, comparator block 24j, arbiter(i) 25i and arbiter(j) 25j.

Please amend paragraph [0047] to read as follows:

[0047] The bank j flag bit information is FBU(j)=0, FBD(j)=1, enables comparator block(j) 24j and compares the incoming Normal access bank (BA) address on line [[18A]] 16A with the fixed refresh bank address ~~Address~~ (RBA) on line 14A as explained above in connection with FIG. 4. The result (output) which is a YES/NO signal on line 44j from comparator block(i) 24j is input to Arbiter(j) 25j.

Please amend paragraph [0048] to read as follows:

[0048] 3. The arbiter(j) 25j is also enabled by the input signal combinations, FBU(j)=0 and FBD(j)=1 on line 75 from step 74 in the program and receives the comparator output j on line 44j and generates a conflict signal on line [[62j]] 62O as an output from the arbiter 25j which is supplied as an input to the arbiter 25i. Arbiter 25i provides a mode select (i) output on line 26i to ROW ADD MUX (i) 23i and the shift input to FBU(i) 21i; and arbiter 25j provides a mode select output on line 26j to ROW ADD MUX (j) 23j and the shift input to FBU(j) 22j as explained in connection with generic arbiter [[26]] 25 in FIG. 5, [[6.]] which provides a generic output on MODE SEL line 26. If the output from comparator block 24j is "YES", the mode select j signal transmitted on line 26j is "1" which shifts FBD(0)...(n-1) by 1 bit upward from LSB to MSB on line 75j to line 75.

Please amend paragraph [0050] to read as follows:

[0050] This keeps the Mode select j on shift line 26j to the FBD(j) 22j at "0" on line 75j to line 75 and does not change the register pattern FBD(0)...(n-1).

Please amend paragraph [0051] to read as follows:

[0051] 4. Arbiter(i) 25i is enabled by the input signal combinations, FBU(i)=1 and FBD(i)=0 on line 75 and receives an output from comparator block(i) 24i on line 44i and the conflict signal from arbiter(j) 25j on line [[62j]] 62O as inputs.

Please amend paragraph [0052] to read as follows:

[0052] If the output from comparator block(i) 24i on line 44i [[iI]] is "YES" and the conflict signal on line [[62j]] 62O is "1", the Mode select(i) output on line 26i from arbiter(i) 25i is "1" supplied on mode select (i) line 26i to FBU(I) 21i, which is a shift signal into FBU(n-1)...FBU(0) by 1 bit downward from MSB to LSB.

Please amend paragraph [0053] to read as follows:

[0053] If the output of comparator block [[24 i]] 24i is "NO", then the Mode select(i) value on line 26i from arbiter(i) 25i is "0"

Please amend paragraph [0056] to read as follows:

[0056] Following the bank selection algorithm above, in multiple n banks, any 1 out of n (1/n) bank is busy for normal access but [[n-1]] (n-1) out of n banks (n-1/n) are idle for refresh at the first cycle. Next cycle, 1/n bank is busy but [[n-2]] (n-2) out of [[n-1]] (n-1) (n-2/n-1) is idle for refresh. At [[n-1]] the (n-1) cycle, any 1/n bank is busy and 1 out of 2 is idle for refresh. Finally, only one bank is not refreshed yet, after [[n-1]] (n-1) cycles. The refresh scheduler book unit 13 handles memory bank selection effectively while reducing complexity from the refresh scheduler book unit 13.

Please amend paragraph [0057] to read as follows:

[0057] The arbiters 25i/25j [[205]] mediate[[s]] the conflict between two candidate banks and decides which bank is to be refreshed. The arbitration is done through two flag bit information and common conflict signals. The comparator results of two candidate banks are shared through arbiters 25i/25j connected to receive signals on common conflict signal[[s on]] out line 62O. When two candidate banks are available for a refresh operation, one of two banks is selected through arbitration following the given priority. In accordance with this invention, the priority is given to the bottom side bank. The "bottom side" refers to the bank FBD(j)=1 and FBU(j) =0, i.e. searched from bank "0". The "upper side" refers to the bank that has FBD(j)=0 and FBU(j) =0, i.e. searched from bank "n-1".

Please amend paragraph [0058] to read as follows:

[0058] In FIG.2B, all of the key components of the refresh scheduler book unit 13 are distributed to each bank i, j, etc.. Only the communication channels, such as conflict signal and bank address are distributed over all memory banks.

Please amend paragraph [0059] to read as follows:

[0059] FIG.7 shows an alternative to the embodiment of FIG.2B that is similar to FIG.1. All of the key components of the refresh scheduler book unit 713 in FIG.2 except Row Address MUX 23 are collected into one place in the refresh scheduler book unit 713 and only a selected refresh bank address [[714B]] 714A is sent to each bank 19X, 19Y and 19Z together with access bank address on line 716A. The refresh scheduler book unit 713 is connected to RBA line 714A, BA line 716A, RA line 716B, and MODE SEL line 726, which are connected to Row Add MUX unit 723, among others. The ROW ADD MUX unit 23 is associated with Row Decoder 727 and WL Driver 728 and BANK (n-1) 19Z, that are analogous to the row address decoder 27, the wordline driver 28 and the BANK (n-1) 19Z in FIG. 2B. FIG. 7 also shows the additional banks Bank (32) 19Y and Bank (0) as part of an array of banks, as indicated by the dotted lines therebetween.

Please amend paragraph [0060] to read as follows:

[0060] FIG. 8 shows an alternative of the embodiment of FIG.2B. All of the key components of the refresh scheduler book unit 813 (as with the refresh scheduler book unit 13 in FIG.2) including RAC 31 are collected into one place in the refresh scheduler book unit 813 and the selected refresh bank address (RBA) 814A and refresh row address (RRA) 814B are sent to each bank 19X, 19Y and 19Z together with normal address 816B and bank address on line 816A. Refresh scheduler book unit 813 is connected to RBA line 814A, RRA line 814B, BA line 816A, and RA line 816B, that are connected to Row Decoder 827, among others. Row Decoder 827 is associated with WL Driver 828 and BANK (n-1) 19Z. FIG. 8 also shows the additional banks Bank (32) 19Y and Bank (0) as part of an array of banks, as indicated by the dotted lines therebetween.

Please amend paragraph [0061] to read as follows:

[0061] FIG. 9A shows a circuit diagram 25 embodying the arbiter 25i of FIG. 6D for the bank (i) of the DRAM memory device of this invention.

Please amend paragraph [0062] to read as follows:

[0062] FIG. 9B shows a conflict signal generator 162 which is a component of each generic arbiter 25 of FIGS. 5 and 9A (separate from the arbiter 25 of FIG. 9A for convenience of illustration) comprising a CMOS pair of PMOS and NMOS transistors P1/N1. A "conflict out" signal is received on line [[62OUT]] 62O (from any one of the arbiters of the DRAM memory) at the gate electrode of the NMOS transistor N1 of arbiter 25i of FIG. 6D from an arbiter 25j in FIG. 6D of the previous bank "j".

Please amend paragraph [0063] to read as follows:

[0063]A global "conflict in" signal is provided at the common drain node on line [[62IN]] 62I as the output between the PMOS and NMOS transistors of the CMOS pair which is to be supplied to [[the]] a next lowest arbiter [[25h]] which is not shown in FIG. 6D, for convenience of illustration. The source of the PMOS transistor P1 is connected to power supply voltage Vdd. The source of the NMOS transistor N1 and the gate of the PMOS transistor P1 are connected to ground.

Please amend paragraph [0065] to read as follows:

[0065] Signal FBD(i) on line 41 and inverted signal FBU(i) on line 42 from inverter IN1 are the two inputs to [[2]] a two input NAND gate NA3, the output of which is inverted by inverter IN7. The output of inverter IN7 together with comparator result(i) on line 44i are the two inputs to two input NAND gate NA4. The NAND gate NA4 generates an output which is inverted by an inverter IN8, which produces a conflict output(i) signal on line 62O [[62OUT]] as well as an input to a two input NOR gate NOR2.

Please amend paragraph [0066] to read as follows:

[0066] The conflict output(i) signal on line 62O [[62OUT]] from IN8 (just described above) and the output of NAND gate NA3 which has been inverted twice by inverters IN7 and IN9 are the two inputs to the two input NOR gate NOR2. [[and]] The output of the NOR gate NOR2 is inverted by an inverter IN10, which provides one of two inputs to a NAND gate NA5, which decides whether Mode SEL(i) is "0 or "1".

Please amend paragraph [0067] to read as follows:

[0067] On the other hand, the input signal FBU(i) on line 41 and ~~inverted~~ the input signal FBD(i) on line 41, which has been inverted via inverter IN6 are two inputs to [[2]] another two input NAND gate [[Gate]] NA1, which supplies an input to inverter IN2. The output of inverter IN2, which on the one hand is inverted by inverter IN4, supplies one input to a three input NOR gate NOR1. On the other hand the output of inverter IN2 together with comparator result(i) on line 44i are inputs to NAND gate NA2 which provides an output that is inverted by inverter IN3 which provides another input to the three input NOR gate NOR1. ~~and the~~ The "conflict in" line 62I ~~62 IN are~~ from the conflict signal generator 162 in FIG. 9A is a third input to NOR gate NOR1. ~~and the~~ The output of the three input NOR gate NOR1 [[which]] passes through inverter IN5 to the other input to two input NAND gate NA5, which, as stated above, decides the Mode SELECT(i) output on line 26i.

Please amend paragraph [0068] to read as follows:

[0068] Referring to the conflict signal generator 162 shown in FIG. 9B, the conflict out(i) signal on line 62O [[62OUT]] from inverter IN8 in FIG. 9A is connected to the gate of NFET N1 and generates the "conflict in" signal on line [[62IN]] 62I in FIGS. 9A and 9B which is a global signal and input to [[3]] the three input NOR gate NOR1.